

CLAIMS

1 1. A method comprising:

2 selecting one of a plurality of debugging modes as a
3 function of a current operating mode of a processor.

1 2. The method of claim 1 further comprising raising an
2 exception after executing an instruction.

1 3. The method of claim 1 further comprising invoking an
2 emulation mode of the processor after executing an
3 instruction.

1 4. The method of claim 1 wherein selecting the debugging
2 mode comprises selecting a first debugging mode when the
3 operating mode comprises user mode, and selecting a second
4 debugging mode when the operating mode comprises supervisor
5 mode.

1 5. A method comprising:

2 receiving an instruction;

3 receiving a signal;

4 selecting a mode of debugging as a function of the
5 signal, wherein selecting the debugging mode comprises

6 selecting a first debugging mode when the signal is a first
7 signal, and selecting a second debugging mode when the
8 signal is a second signal; and
9 executing the instruction.

1 6. The method of claim 5 further comprising raising an
2 exception.

1 7. The method of claim 5 further comprising invoking an
2 emulation event.

1 8. The method of claim 5 further comprising:
2 sensing register contents; and
3 outputting register contents.

1 9. The method of claim 5, wherein the instruction is
2 received by a processor adapted to operate in a plurality
3 of states, the method further comprising:
4 sensing states of the processor; and
5 outputting states of the processor.

1 10. The method of claim 5, wherein the instruction is
2 received by a processor, the method further comprising

3 selecting a mode of single-step debugging as a function of
4 the operating mode of the processor.

1 11. A device comprising:

2 a processor, the processor adapted to operate in a
3 plurality of operating modes including an emulation mode;
4 a control register adapted to store the state of a
5 control bit; and
6 an exception handler;

7 wherein the processor is adapted to select one of a
8 plurality of debugging modes as a function of the control
9 bit.

1 12. The device of claim 11, wherein the processor is
2 adapted to select one of a plurality of debugging modes as
3 a function of the current operating mode of the processor.

1 13. The device of claim 11, further comprising exception
2 logic adapted to sense the state of the control bit and to
3 trigger an exception event as a function of the state of
4 the control bit.

1 14. The device of claim 11, further comprising emulation
2 logic adapted to sense the state of the control bit and to

3 trigger an emulation event as a function of the state of
4 the control bit.

1 15. The device of claim 11, wherein the control bit is a
2 first control bit, the system further comprising a second
3 control bit, and wherein the mode of single-step debugging
4 is a function of the state of the second control bit.

1 16. The device of claim 11, wherein the processor is a
2 digital signal processor.

1 17. A device comprising:
2 a processor, the processor adapted to operate in a
3 plurality of operating modes;
4 wherein the processor is adapted to select one of a
5 plurality of debugging modes as a function of the current
6 operating mode of the processor.

1 18. The device of claim 17 further comprising a control
2 register adapted to store the state of a control bit,
3 wherein the processor is adapted to select one of the
4 plurality of debugging modes as a function of the state of
5 the control bit.

1 19. The device of claim 18, further comprising:
2 an exception handler; and
3 logic adapted to sense the state of the control bit
4 and to trigger an exception event as a function of the
5 state of the control bit.

1 20. The device of claim 18, further comprising logic
2 adapted to sense the state of the control bit and to
3 trigger an emulation event as a function of the state of
4 the control bit.

1 21. The device of claim 17, wherein the processor is a
2 digital signal processor.

1 22. A system comprising:
2 a processor, the processor adapted to operate in a
3 plurality of operating modes;
4 a control register adapted to store the state of a
5 control bit;
6 an input/output device; and
7 an exception handler;
8 wherein the processor is adapted to select one of a
9 plurality of debugging modes as a function of the control
10 bit.

1 23. The system of claim 22, wherein the processor is
2 adapted to select one of a plurality of debugging modes
3 based upon the current operating mode.

1 24. The system of claim 22, further comprising a memory
2 device coupled to the processor.

1 25. The system of claim 22, further comprising logic
2 adapted to sense the state of the control bit and to
3 trigger an exception event as a function of the state of
4 the control bit.

1 26. The system of claim 22, further comprising logic
2 adapted to sense the state of the control bit and to
3 trigger an emulation event as a function of the state of
4 the control bit.

1 27. The system of claim 22, wherein the control bit is a
2 first control bit, the system further comprising a second
3 control bit, wherein the processor is adapted to select one
4 of a plurality of debugging modes based upon the state of
5 the second control bit.